IN THE SPECIFICATION:

Please revise the specification as follows:

Please amend the paragraph starting on page 4, line 28 as follows:

As discussed below, the MTDCLK signal is a phase adjusted system clock signal for a selected slave device 24. The MTDCLK signal is synchronized to transmit data, such that the selected slave device of the master/slave system 20 receives the data in phase with the system clock. The MTDCLK signal accounts for the time between launching data from the master 24 22 to the time that it is received at the slave 24. This time difference, expressed as a phase difference between the system clock and the MTDCLK, allows the master device 22 to launch data in a manner such that it is received at a selected slave device 24 in phase with the system clock.

